In re the application of:

WARREN M. FARNWORTH ALAN G. WOOD TRUNG TRI DOAN

Serial No. 10/646,897

Examiner: LEWIS, MONICA

Filed: **08-22-2003**

Art Unit: 2822

Title: SEMICONDUCTOR COMPONENT HAVING THINNED

DIE WITH CONTACT BUMPS AND POLYMER LAYERS

ON SIX SIDES (AS AMENDED)

Docket No. 01-1059.01

INFORMATION DISCLOSURE STATEMENT (IDS) UNDER 37 CFR 1.97 February 9, 2007

Mail Stop RCE Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Applicants submit herewith patents, publications or other information which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 CFR 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR 1.97(g) the filing of this Information Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists.

The attached form, PTO SB/08, provides a listing of patents, publications, or other information as required by 37 CFR 1.98(a)(1).

This Information Disclosure Statement is being submitted with only copies of on-US patent publication(s) and non-patent literature. This protocol conforms with 37 CFR 1.98(a)(2)(i), which waives the requirement for submitting a copy of each cited US patent and each US patent application publication for all US national patent applications filed after June 30, 2003.

With respect to patents JP 2000-31185 and JP 10-79362, the following concise statement of relevance is herein submitted by the undersigned.

JP 2000-31185 discloses in Figures 1a-1i a process wherein a semiconductor substrate 1 is thinned from a thickness of t1 in Figure 1a to t2 in Figure 1h. This reference is relevant because claim 170 of the present application claims a semiconductor component having a "thinned die".

JP 10-79362 discloses in Figures 41a-41c a process wherein a semiconductor substrate 16 includes trenches 105 containing a material 13, which are cut along cut lines x forming edge polymer layers. This reference is relevant because claim 265 of the present application claims a semiconductor component having an edge polymer layer which comprises a portion of a polymer filled trench.

DATED this 9th day of February, 2007.

Respectfully submitted:

ratton, Reg No. 28,418

Attorney of Record

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CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, PO BOX 1450, Alexandria, VA 22313-1450 on this 9th day of February, 2007.

en A. Gratton, Attorney for Applicants

PTO/SB/08A (09-06) Approved for use through 03/31/2007. OMB 0651-0031

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Substitute for form 1449/PTO

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

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Application Number	10/646,897		
Filing Date	08-22-2003		
First Named Inventor	WARREN M. FARNWORTH		
Art Unit	2822		
Examiner Name	LEWIS, MONICA		
Attorney Docket Number	01-1059 01		

			U. S. PATEN	T DOCUMENTS	
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ^{2 (f known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	Α	^{US-} 2005/0168908	08-04-2005	Maeda et al.	
	В	^{US-} 7,157,353 B2	01-02-2007	Farnworth et al.	
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Examiner Initials*	Cite No.1	Foreign Patent Document Country Code ³ Number ⁴ Kind Code ⁵ (if known)	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	
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	D	JP 10-79362	03-24-1998			
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Examiner	Date	
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		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	E	PETER VAN ZANT, Microchip Fabrication, 2000, McGraw-Hill, Fourth Edition, page 588.	
			
Examiner	· · · · · ·	Date	
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